Amendment to Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (Currently amended) The integrated circuit of claim ~~1~~8, further comprises a second electrode formed on the ferroelectric layer opposite of the first electrode.

3. (Currently amended) The integrated circuit of claim ~~1~~8, wherein the spacer comprises of an insulation material.

4. (Currently amended) The integrated circuit of claim ~~1~~8, wherein the ferroelectric layer comprises of a polymer.

5. (Currently amended) The integrated circuit of claim ~~1~~8, wherein the support surface comprises of insulation material.

6. (Currently amended) The integrated circuit of claim ~~1~~8, wherein a portion of the spacer nearest to the first electrode surface has a height about equal to a height of the first electrode, the height of the first electrode being a distance between the support surface and a second electrode surface of the first electrode, the second electrode surface being substantially parallel to the support surface.

7. (Currently amended) The integrated circuit of claim ~~1~~8, wherein the spacer is in contact with the first electrode surface.

8. (Currently amended) ~~The~~An integrated circuit ~~of claim 1~~, comprising:
a first electrode formed on a support surface, the first electrode having a first electrode surface that intersects the support surface;
a spacer positioned on the support surface adjacent to the first electrode surface, wherein the spacer is separated from the first electrode surface; and
a ferroelectric layer formed on the first electrode and the spacer.

9. (Currently amended) The integrated circuit of claim ~~1~~8, wherein the support surface is located on a die.

10. (Cancelled)

11. (Currently amended) The integrated circuit of claim ~~1~~8, wherein the first electrode comprises first and second portions, the first portion comprising a first material that is non-reactive to the ferroelectric layer and located at a second electrode surface of the first electrode, the second electrode surface being parallel to the support surface, and the second portion comprising a second material that is more conductive than said first material and located between the first portion and the support surface.

12. (Cancelled)

13. (Withdrawn) A method, comprising:
forming a first electrode on a support surface, the first electrode having a first electrode surface that intersects the support surface;
forming a spacer positioned on the support surface adjacent to the first electrode surface; and
forming a ferroelectric layer on the first electrode and the spacer.

14. (Withdrawn) The method of claim 13, further comprises forming a second electrode on the ferroelectric layer opposite of the first electrode.

15. (Withdrawn) The method of claim 13, wherein said forming of a spacer comprises forming a portion of the spacer nearest to the first electrode surface with a height about equal to a height of the first electrode, the height of the first electrode being a distance between the support surface and a second electrode surface of the first electrode, and the second electrode surface being substantially parallel to the support surface.

16. (Withdrawn) The method of claim 13, wherein said forming of a spacer comprises forming the spacer by plasma enhanced chemical vapor deposition.

17. (Withdrawn) The method of claim 13, wherein said forming of a spacer comprises forming the spacer by depositing a spacer material on and around the first electrode and removing spacer material from a second electrode surface of the first electrode that is parallel to the support surface.

18. (Withdrawn) The method of claim 17, wherein the removing of the spacer material from the second electrode surface comprises removing the spacer material by a selected one of dry and wet etch.

19. (Withdrawn) The method of claim 13, wherein said forming of a spacer comprises forming the spacer for a selected one of moving a transition point away from the first electrode and reducing sharpness of a transition.

20. (Withdrawn) The method of claim 13, wherein said forming of a ferroelectric layer comprises forming the ferroelectric layer by spincoating.

21. (Withdrawn) A system, comprising:

an integrated circuit, including

a first electrode formed on a support surface, the first electrode having a first electrode surface that intersects the support surface,

a spacer positioned on the support surface adjacent to the first electrode surface, and

a ferroelectric layer formed on the first electrode and the spacer;

a bus coupled to the integrated circuit; and

a networking interface coupled to the bus.

22. (Withdrawn) The system of claim 21, wherein the integrated circuit further comprises a second electrode formed on the ferroelectric layer opposite of the first electrode.

23. (Withdrawn) The system of claim 21, wherein the spacer comprises an insulation material.

24. (Withdrawn) The system of claim 21, wherein the ferroelectric layer comprises a polymer.

25. (Withdrawn) The system of claim 21, wherein the support surface comprises an insulation material.

26. (Currently amended) The integrated circuit of claim ~~1~~8, wherein the integrated circuit is a memory circuit.

27. (Previously presented) The integrated circuit of claim 26, wherein the integrated circuit is a non-volatile memory circuit.

28. (Previously presented) The integrated circuit of claim 2, wherein the second electrode adaptedly formed on the ferroelectric layer opposite the first electrode to form a memory cell.

29. (Withdrawn) The system of claim 21, wherein the integrated circuit is a memory circuit.

30. (Withdrawn) The integrated circuit of claim 29, wherein the integrated circuit is a non-volatile memory circuit.

31. (Withdrawn) The integrated circuit of claim 22, wherein the second electrode adaptedly formed on the ferroelectric layer opposite of the first electrode to form a memory cell.

32. (New) An integrated circuit, comprising:

a first electrode formed on a support surface, the first electrode having a first electrode surface that intersects the support surface and a second electrode surface that is substantially parallel to the support surface;

a spacer positioned on the support surface adjacent to the first electrode surface, the spacer having a first spacer surface that is substantially parallel to the support surface and includes a transition point, wherein the spacer is positioned to create a separation distance between the first electrode and the transition point, such that the first spacer surface is substantially in a same plane as the second electrode surface; and

a ferroelectric layer formed on the first electrode and the spacer.

33. (New) The integrated circuit of claim 32, further comprises a second electrode formed on the ferroelectric layer opposite of the first electrode.

34. (New) The integrated circuit of claim 32, wherein the spacers are in contact with the first electrode surface.

35. (New) The integrated circuit of claim 32, wherein the first electrode comprises first and second portions, the first portion comprising a first material that is non-reactive to the ferroelectric layer and located at a second electrode surface of the first electrode, the second electrode surface being parallel to the support surface, and the second portion comprising a second material that is more conductive than said first material and located between the first portion and the support surface.

36. (New) The integrated circuit of claim 35, wherein the spacer is formed against the first electrode surface such that the spacer isolates the second portion from the ferroelectric layer.

37. (New) The integrated circuit of claim 32, wherein the integrated circuit is a memory circuit.

38. (New) The integrated circuit of claim 37, wherein the integrated circuit is a non-volatile memory circuit.

39. (New) The integrated circuit of claim 33, wherein the second electrode adaptedly formed on the ferroelectric layer opposite the first electrode to form a memory cell.

40. (New) An integrated circuit, comprising:

at least two first electrodes, wherein the first electrodes are formed on a support surface, the first electrodes having first electrode surfaces that intersect the support surface;

a gap region between the first electrode surfaces;

a spacer on the support surface in the gap region, wherein the gap region is substantially occupied by the spacer; and

a ferroelectric layer formed on the first electrodes and the spacer.

41. (New) The integrated circuit of claim 40, further comprises second electrodes formed on the ferroelectric layer opposite each of the first electrodes.

42. (New) The integrated circuit of claim 40, wherein portions of the spacer nearest to the first electrode surfaces have a height about equal to a height of the first electrodes, the height of the first electrodes being a distance between the support surface and second electrode surfaces of the first electrodes, the second electrode surfaces being substantially parallel to the support surface.

43. (New) The integrated circuit of claim 41, wherein the second electrodes adaptedly formed on the ferroelectric layer opposite the first electrodes to form memory cells.